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data and common electrodes parallel to the data bus line in the pixel region, the data and common electrodes having portions for first and second storage capacitors;

a passivation layer over the thin film transistor and the data electrode, wherein the common electrode is formed on the passivation layer parallel to the data electrode and overlapping the gate and data bus lines; and

a first alignment layer over the common electrode.

34. (New) The in-plane switching mode liquid crystal display of claim 33, further comprising a black mask and a color filter on a second substrate opposite to the first substrate.

35. (New) The in-plane switching mode liquid crystal display of claim 34, wherein the black mask includes one of a Cr and a CrOx metal layer.

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36. (New) The in-plane switching mode liquid crystal display of claim 35, wherein the metal layer has a thickness of about 0.1 μm and a width of about 10 μm.

37. (New) The in-plane switching mode liquid crystal display of claim 34, further comprising a second alignment layer on the color filter layer.

38. (New) The in-plane switching mode liquid crystal display of claim 37, wherein the second alignment layer includes one of polyimide and photo-alignment materials.

39. (New) The in-plane switching mode liquid crystal display of claim 34, further comprising a liquid crystal layer between the first and second substrates.

40. (New) The in-plane switching mode liquid crystal display of claim 33, further comprising gate, data, and common pads connected to driving circuits.

41. (New) The in-plane switching mode liquid crystal display of claim 40, wherein the gate and data bus lines are connected to the driving circuits.

42. (New) The in-plane switching mode liquid crystal display of claim 40, wherein the common

bus line is grounded through the common pad.

43. (New) The in-plane switching mode liquid crystal display of claim 40, wherein the gate, data and common pads include first, second and third metal layers, respectively.

44. (New) The in-plane switching mode liquid crystal display of claim 43, wherein the first metal layers includes Mo/Al double metal layers together with the gate electrode and common bus line.

45. (New) The in-plane switching mode liquid crystal display of claim 43, wherein the second metal layer includes Cr together with the source and drain electrodes.

46. (New) The in-plane switching mode liquid crystal display of claim 43, wherein the third metal layer includes indium tin oxide together with the common electrode.

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47. (New) The in-plane switching mode liquid crystal display of claim 33, further comprising a grounding wiring connected to the gate and data bus lines through an electrostatic shielding circuit.

48. (New) An in-plane switching mode liquid crystal display comprising:

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gate and data bus lines on a first substrate defining a pixel region;

a common bus line parallel to the gate bus line;

a thin film transistor at a crossing of the gate and data bus lines, the thin film transistor having a gate electrode, a gate insulator, a semiconductor layer, a source electrode, and a drain electrode;

data and common electrodes parallel to the data bus line in the pixel region, wherein the common electrode has first and second oblique sides;

a passivation layer over the thin film transistor and the data electrode; and

a first alignment layer over the common electrode.

49. (New) The in-plane switching mode liquid crystal display of claim 48, wherein the first

oblique side is inclined counterclockwise to an X axis direction with an angle θ_A.

50. (New) The in-plane switching mode liquid crystal display of claim 48, wherein the second oblique side is inclined clockwise to an X axis direction with an angle θ_B.

51. (New) The in-plane switching mode liquid crystal display of claim 49, wherein an alignment direction is inclined counterclockwise to an X axis direction with an angle θ_R.

52. (New) The in-plane switching mode liquid crystal display of claim 50, wherein an alignment direction is inclined counterclockwise to an X axis direction with an angle θ_R.

53. (New) The in-plane switching mode liquid crystal display of claim 51, wherein the range of θ_R is about 0° to 90°.

B11 54. (New) The in-plane switching mode liquid crystal display of claim 52, wherein the range of θ_R is about 0° to 90°.

55. (New) The in-plane switching mode liquid crystal display of claim 53, wherein the range of θ_A is about θ_R to 90°.

56. (New) The in-plane switching mode liquid crystal display of claim 54, wherein the range of θ_B is about 90°- θ_R to 90°.

57. (New) The in-plane switching mode liquid crystal display of claim 49, wherein θ_A is about 45°.

58. (New) The in-plane switching mode liquid crystal display of claim 50, wherein θ_B is about 45°.

59. (New) The in-plane switching mode liquid crystal display of claim 51, wherein θ_R is about 75°.

60. (New) The in-plane switching mode liquid crystal display of claim 52, wherein θ_R is about 75°.

61. (New) The in-plane switching mode liquid crystal display of claim 48, wherein the common electrode is formed on the passivation layer.

62. (New) The in-plane switching mode liquid crystal display of claim 48, wherein the common electrode overlaps the gate and data bus lines.

63. (New) The in-plane switching mode liquid crystal display of claim 48, wherein the data and common electrodes have portions for first and second storage capacitors.

64. (New) An in-plane switching mode liquid crystal display comprising:

gate and data bus lines on a first substrate defining a pixel region;

a common bus line parallel to the gate bus line;

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a thin film transistor at a crossing of the gate and data bus lines, the thin film transistor having a gate electrode, a gate insulator, a semiconductor layer, a source electrode, and a drain electrode;

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data and common electrodes parallel to the data bus line in the pixel region;

a passivation layer over the thin film transistor and the data electrode, wherein the common electrode is formed on the passivation layer parallel to the data electrode;

a light shielding layer on the passivation layer; and

a first alignment layer over the common electrode.

65. (New) The in-plane switching mode liquid crystal display of claim 64, wherein the common electrode and the light shielding layer include Mo and indium tin oxide.

66. (New) The in-plane switching mode liquid crystal display of claim 65, wherein the thickness of the Mo is about 1000Å.

67. (New) The in-plane switching mode liquid crystal display of claim 64, wherein the light shielding layer overlaps a portion of the gate bus line through a hole in the gate insulator and the

passivation layer.

68. (New) The in-plane switching mode liquid crystal display of claim 64, wherein the data and common electrodes have portions for first and second storage capacitors.

69. (New) An in-plane switching mode liquid crystal display comprising:

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gate and data bus lines on a first substrate defining a pixel region;

a common bus line parallel to the gate bus line;

a thin film transistor at a crossing of the gate and data bus lines, the thin film transistor having a gate electrode, a gate insulator, a semiconductor layer, a source electrode, and a drain electrode;

data and common electrodes parallel to the data bus line in the pixel region;

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a passivation layer over the thin film transistor and the data electrode, wherein the common electrode is formed on the passivation layer parallel to the data electrode and overlaps the gate and data bus lines;

a light shielding layer on the passivation layer; and

a first alignment layer over the common electrode.

70. (New) The in-plane switching mode liquid crystal display of claim 69, wherein the common electrode and the light shielding layer include opaque materials.

71. (New) The in-plane switching mode liquid crystal display of claim 69, wherein the data and common electrodes have portions for first and second storage capacitors.--